LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A MOSgated semiconductor device comprising:

a ~~channel~~ trench receiving region of a first conductivity type having a top first surface;

a common channel region of a second conductivity type formed in said ~~channel~~ trench receiving region and extending to a first depth below said top first surface;

a plurality of spaced trenches formed in said ~~channel~~ trench receiving region through said common channel region;

a first region of a first conductivity type formed at the bottom of each trench, each said first region of said first conductivity type being adjacent to said ~~channel~~ trench receiving region and of a higher conductivity than said ~~channel~~ trench receiving region;

a plurality of conductive regions of said first conductivity type each disposed adjacent a trench; ~~and~~

a contact layer formed over said channel receiving region and in ohmic contact with said plurality of ~~contact~~ conductive regions; and field relief regions of said second conductivity type formed in said trench receiving region below said first depth, wherein said field relief regions are spaced from said channel region.

2.-3. Canceled

4. (Currently Amended) A device according to claim 1, wherein said ~~channel~~ trench receiving region is an epitaxial layer of semiconductive material formed over a substrate.

5. (Original) A device according to claim 4, further comprising a second contact formed over said substrate.

6. (Original) A device according to claim 5, wherein said second contact is a trimetal contact.

7. (Original) A device according to claim 1, further comprising high conductivity contact regions of said second conductivity type formed in said channel region and in ohmic contact with said contact layer.

8. (Original) A device according to claim 1, wherein said conductive regions are source regions.

9. (Original) A device according to claim 1, wherein each of said trenches is filled with a conductive material and lined at each side wall thereof with a gate insulation material.

10. (Currently Amended) A MOSgated semiconductor device comprising:

a semiconductor die having an epitaxial layer of a first conductivity type formed over a substrate;

a channel region of a second conductivity type formed in said epitaxial layer;

a plurality of spaced trenches formed in said epitaxial layer;

a first region of a first conductivity type formed at the bottom of each trench, each said first region of said first conductivity type being adjacent to said epitaxial layer and of a higher conductivity than said epitaxial layer;

a plurality of source regions of said first conductivity type each disposed adjacent a trench; ~~and~~

a source contact formed over said epitaxial layer and in ohmic contact with said plurality of ~~contact~~ source regions; and field relief regions of said second conductivity type formed below said channel region, conductivity of said first regions of said first conductivity type and said field relief regions being selected to create a superjunction in said device.

11. Canceled.

12. (Original) A device according to claim 11, wherein said field relief regions are spaced from said channel region.

13. (Currently Amended) A device according to claim 10, wherein said substrate is a semiconductive material of the same conductivity type as said epitaxial layer but of ~~lower~~ higher conductivity.

14. (Original) A device according to claim 13, further comprising a drain contact formed over said substrate.

15. (Currently Amended) A device according to claim 14, wherein said ~~second~~ drain contact ~~is~~ comprises a trimetal contact.

16. (Original) A device according to claim 10, further comprising high conductivity contact regions of said second conductivity type formed in said channel region and in ohmic contact with said source contact.

17. (Original) A device according to claim 10, wherein each of said trenches is filled with a conductive material and lined at each side wall thereof with a gate insulation material.

18. (Original) A device according to claim 17, wherein said conductive material is polysilicon and said gate insulation material is oxide.

19. (Original) A device according to claim 1, wherein said trenches extend to a depth below said channel region.

20. (Original) A device according to claim 17, wherein said trenches extend to a depth below said channel region.